What is claimed is:

[Claim 1] 1. A method of fabricating a semiconductor structure, comprising:

providing a substrate;

forming a dielectric layer on a top surface of said substrate;

forming a polysilicon layer on a top surface of said dielectric layer;

implanting said polysilicon layer with N-dopant species, said N-dopant species about contained within said polysilicon layer;

implanting said polysilicon layer with a nitrogen containing species, said nitrogen containing species about contained within said polysilicon layer.

[Claim 2] 2. The method of claim 1, wherein a peak concentration of said N-dopant species is about equal to a peak concentration of said nitrogen containing species at about a same distance from a top surface of said polysilicon layer.

[Claim 3] 3. The method of claim 1, wherein a surface concentration of said N-dopant species is about equal to a surface concentration of said nitrogen containing species at about a same distance from a top surface of said polysilicon layer.

[Claim 4] 4. The method of claim 1, wherein said N-dopant species and said nitrogen containing species have about a same ion implantation concentration profile.

[Claim 5] 5. The method of claim 1, wherein a surface concentration of said N-dopant species is between about 1E18 atm/cm^3 to about 1E22 atm/cm^3 and a surface concentration of said nitrogen containing species is between about abut 1E18 atm/cm^3 to about 1E21 atm/cm^3.

[Claim 6] 6. The method of claim 1, wherein:

wherein a peak concentration of said N-dopant species is between about 1E18 atm/cm^3 to about 1E22 atm/cm^3 and a peak concentration of said nitrogen containing species is between about 1E18 atm/cm^3 to about 1E21 atm/cm^3; and

said peak concentration of said N-dopant species occurring between a distance of about 0 nm and about 1/3 of a thickness of said polysilicon layer from a top surface of said polysilicon layer and said peak concentration of said nitrogen containing species occurring between about 0 nm to about 2/3 of said thickness of said polysilicon layer from said top surface of said polysilicon layer.

[Claim 7] 7. The method of claim 1, wherein:

said N-dopant species is selected from the group consisting of phosphorus and arsenic; and

said nitrogen containing species is selected from the group consisting of N, N_2, NO, NF_3, N_2O and NH_3.

[Claim 8] 8. The method of claim 1, further including:

patterning said polysilicon layer into one or more polysilicon lines;

performing a thermal oxidation of sidewalls and top surfaces of said one or more polysilicon lines to form a thermal oxide layer, said thermal oxide layer of about uniform thickness.

[Claim 9] 9. The method of claim 8, wherein said nitrogen containing species retards oxidation of said one or more polysilicon lines.

[Claim 10] 10. A method of fabricating a semiconductor structure, comprising:

(a) providing a substrate;

(b) forming a dielectric layer on a top surface of said substrate;

(c) forming a polysilicon layer on a top surface of said dielectric layer;

(d) implanting a first portion of said polysilicon layer with N-dopant species, said N-dopant species about contained within said polysilicon layer;

(e) implanting a second and different portion of said polysilicon layer with P-dopant species, said P-dopant species about contained within said polysilicon layer;

(f) implanting said first portion of said polysilicon layer with a nitrogen containing species, said nitrogen containing species essentially contained within said polysilicon layer.

[Claim 11] 11. The method of claim 10, further including:

(g) implanting said second portion of said polysilicon layer with said nitrogen containing species.

[Claim 12] 12. The method of claim 10, wherein a peak concentration of said N-dopant species is about equal to a peak concentration of said nitrogen containing species at about a same distance from a top surface of said polysilicon layer.

[Claim 13] 13. The method of claim 10, wherein a surface concentration of said N-dopant species is about equal to a surface concentration of said nitrogen containing species at about a same distance from a top surface of said polysilicon layer.

[Claim 14] 14. The method of claim 10, wherein said N-dopant species and said nitrogen containing species have about a same ion implantation concentration profile.

[Claim 15] 15. The method of claim 10, wherein a surface concentration of said N-dopant species is between about 1E18 atm/cm^3 to about 1E22 atm/cm^3 and a surface concentration of said nitrogen containing species is between about abut 1E18 atm/cm^3 to about 1E21 atm/cm^3.

[Claim 16] 16. The method of claim 10, wherein:

wherein a peak concentration of said N-dopant species is between about 1E18 atm/cm^3 to about 1E22 atm/cm^3 and a peak concentration of said nitrogen containing species is between about 1E18 atm/cm^3 to about 1E21 atm/cm^3; and

said peak concentration of said N-dopant species occurring between a distance of about 0 nm and about 1/3 of a thickness of said polysilicon layer from a top surface of said polysilicon layer and said peak concentration of said nitrogen containing species occurring between about 0 nm to about 2/3 of said thickness of said polysilicon layer from said top surface of said polysilicon layer.

[Claim 17] 17. The method of claim 10, wherein:

said N-dopant species is selected from the group consisting of phosphorus and arsenic; and

said nitrogen containing species is selected from the group consisting of N, N_2, NO, NF_3, N_2O and NH_3.

[Claim 18] 18. The method of claim 10, further including:

after steps (a) through (f), (g) patterning said first portion of said polysilicon layer into one or more NFET gate electrodes and patterning said second portion of said polysilicon layer into one or more PFET gate electrodes; and

(h) performing a thermal oxidation of sidewalls and top surfaces of said one or more NFET and PFET gate electrodes to form a thermal oxide layer.

[Claim 19] 19. The method of claim 18, wherein said nitrogen containing species retards oxidation of said one or more NFET gate electrodes.

[Claim 20] 20. The method of claim 18, further including:

after step (h), removing said thermal oxide layer from said top surfaces of said NFET and PFET gate electrodes and forming a metal silicide layer on said top surfaces of NFET and PFET gate electrodes.